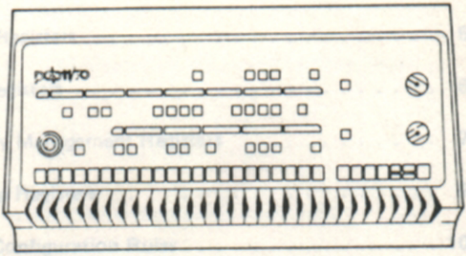
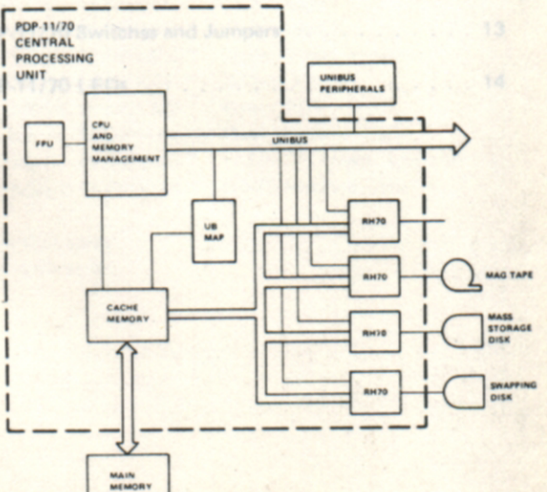
digital

PDP-11/70

MAINTENANCE CARD





11 4550

PDP-11/70 DIAGNOSTICS

Each diagnostic test assumes successful completion of preceding test(s).

Diagnostics should be run in the following sequence; otherwise errors may *not* be detected or if detected may give misleading messages on the console printout.

The PDP-11/70 diagnostics are stored on three disks:

1. MAINDEC-11-DZZZA-*-HB
2. MAINDEC-11-DZZZB-*-HB
3. MAINDEC-11-DZZZC-*-HB

MAINDEC-11-DEKBI-* is a paper tape diagnostic to check the M9301-YC Diagnostic/Terminator.

PDP-11/70 DIAGNOSTIC SEQUENCE

MAINDEC-11-DEKBH-*	Diagnostic ROM (M9301-YC)†
MAINDEC-11-DEKBA-*	CPU, part 1†
MAINDEC-11-DEKBB-*	CPU, part 2
MAINDEC-11-DEKBC-*	Cache, part 1
MAINDEC-11-DEKBD-*	Cache, part 2
MAINDEC-11-DEKBE-*	Memory Management
MAINDEC-11-DEKBF-*	Unibus Map
MAINDEC-11-DEKBG-*	Power Fail
MAINDEC-11-DEMJA-*	Main Memory (MJ11)
MAINDEC-11-DEQKC-*	11/70 CPU Instr. Exerciser
MAINDEC-11-DERHA-*	RH70 Massbus Control

*Revision letter.
†Halts on error.

M9301-YC BOOT PROCEDURE

1. Load address 17765000.
2. Set switch register for the following:*

Drive Number	SWR <02:00>
Device Code	SWR <07:03>
32K Memory Bank	SWR <15:12>

3. Press START.

DEVICE CODES AND DEVICE NAMES

01	TM11/TU10	Magtape, TM11
02	TC11/TU56	DECtape, TC11-G
03	RK11/RK05	DECpack, RK11-D
04	RP11/RP03	Disk Pack, RP11-C
05	Reserved	(HALT)
06	RH70/TU16	Magtape, TWU16
07	RH70/RP04	Disk Pack, RWP04
10	RH70/RS04	Fixed Head Disk, RWS04/03
11	RX11/RX01	Diskette

MEMORY BANK AND PHYSICAL ADDRESS

00	0 – 28K
01	32K – 60K
02	64K – 92K
–	–
16	448K – 476K
17	480K – 508K

NOTE

To boot with cache off, first deposit 14 in the control register (17,777,746).

*To boot without running diagnostic (from Unibus), deposit 173000 into the PC (17777707), set the device code into SWR <07:03> and press CONTINUE.

M9301-YC ERROR HALTS

Halt (PC+2)	Test No.	Failing Instruction(s)
165004	1	Unconditional Branch
165020	2	CLR//BMI/BVS/BHI/BLOS
165036	3	DEC//BPL/BEQ/BGE/BGT/BLE
165052	4	ROR//BVC/BHIS/BHI/BNE
165066	5	SEZ//BHI/BLT/BLOS
165076	6	CLZ//BLE/BGT
165134	7	Register data path and modes 2, 3, 6./sub
165146	10	ROL/BCC/BLT
165166	11	ADD/INC/COM/BCS/BLE
165204	12	ROR/BIS/ADD/BLO/BGE/INC
165214	13	DEC/BLOS/BLT
165222	14	COM
165236	14	BIC/BGT/BGE/BLE
165260	15	ADC/CMP/BIT/BNE/BGT/BEQ
165270	16	MOVB/BPL
165312	16	SOB/CLR/TEST/BNE
165346	17	ASR/ASL
165360	20	ASH
165374	20	ASH/SWAB
165450	21	Kernel PARs
165474	22	Kernel IPDRs
165510	23	JSR
165520	23	Wrong value pushed on stack
165530	23	RTS
165542	23	RTI
165550	23	JMP
(no halt)	24	Load and turn on memory management and Map

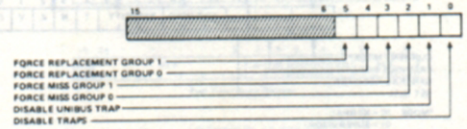
M9301-YC ERROR HALTS (Cont)

Halt (PC+2)	Test No.	Failing Instruction(s)
165742	25	Main memory 1000 – 28K (Cache OFF)
165760	25	Data is not complement of own address
166000	25	Parity error
173644	26	Cache memory error (Cache test)
173654	26	No hits in cache
173736	27	Data compare error (main memory/cache ON
173746	27	No hit; R0 = address
173764	27	Cache error

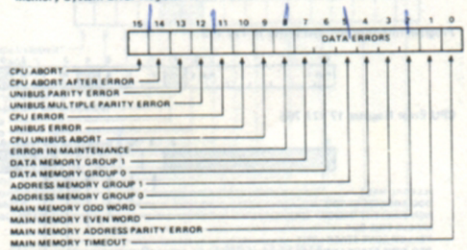
*If error halts in test 26 or 27, press CONTINUE to boot with cache OFF.

CACHE REGISTERS

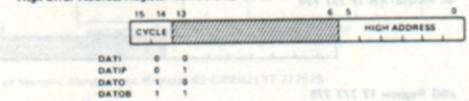
Control Register 17 777 746



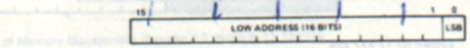
Memory System Error Register 17 777 744



High Error Address Register 17 777 742

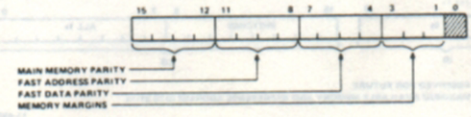


Low Error Address Register 17 777 740



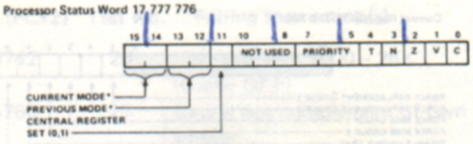
Hit/Miss Register 17 777 752

Maintenance Register 17 777 750

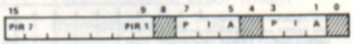


CPU REGISTERS

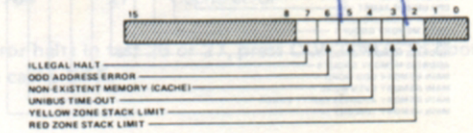
Processor Status Word 17,777 776



Program Interrupt Request (PIR) 17 777 772



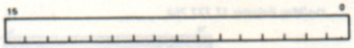
CPU Error Register 17 777 766



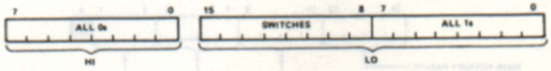
SL REGISTER 17 777 774

μBG Register 17 777 770

System ID 17 777 764



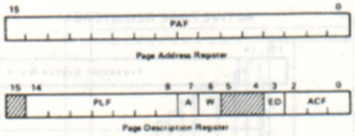
SYSTEM SIZE HI 17 777 762
LO 17 777 760



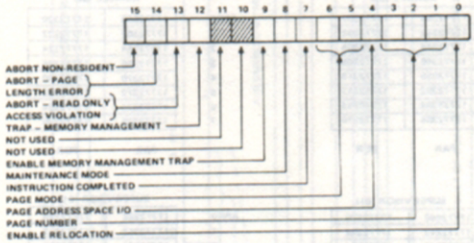
HI = RESERVED FOR FUTURE
SWITCHES = MAXIMUM AVAILABLE MEMORY AND REPRESENTS ADDRESS BITS 21:14

11-4562

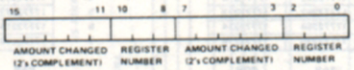
MEMORY MANAGEMENT REGISTERS



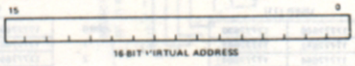
Format of Memory Management Register #0 (MMR0) 17 777 572



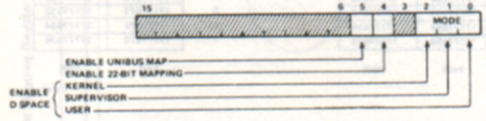
Format of Memory Management Register #1 (MMR1) 17 777574



Format of Memory Management Register #2 (MMR2) 17 777576



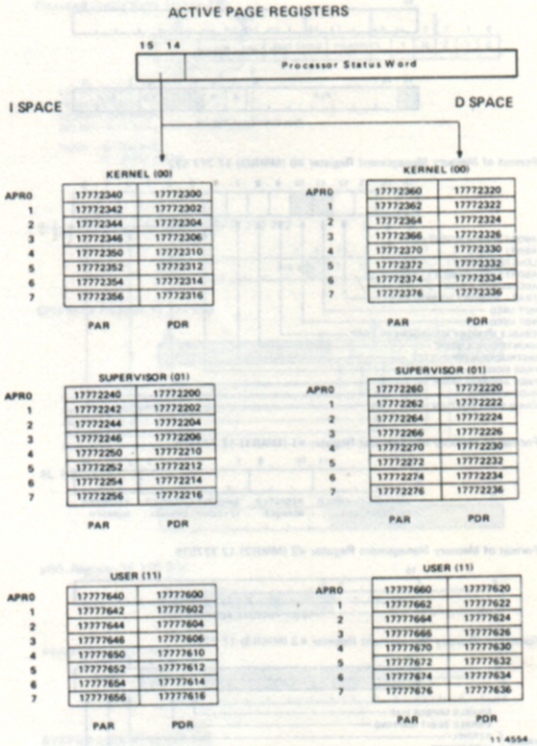
Format of Memory Management Register #3 (MMR3) 17 772516



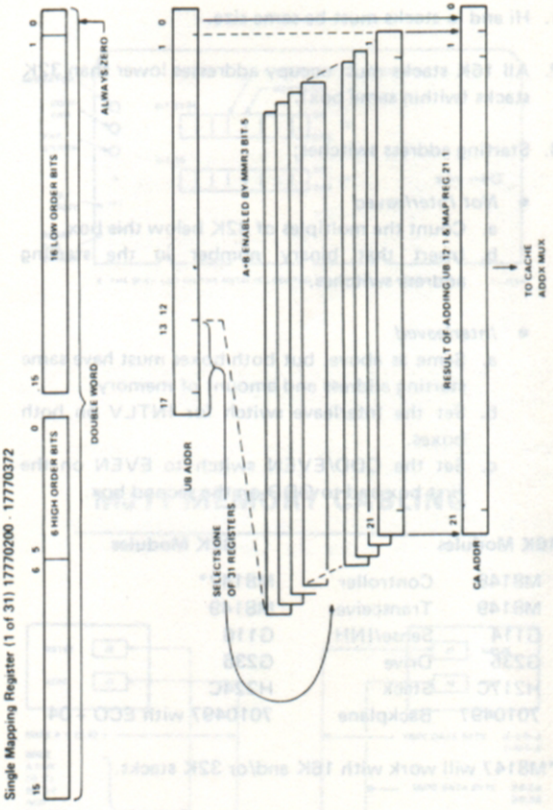
11-4553

MEMORY MANAGEMENT REGISTERS (Cont)

ACTIVE PAGE REGISTERS



UB-MAP REGISTERS



MJ11 MEMORY CONFIGURATION RULES

1. Hi and lo stacks must be same size.

2. All 16K stacks must occupy addresses lower than 32K stacks (within same box).

3. Starting address switches:

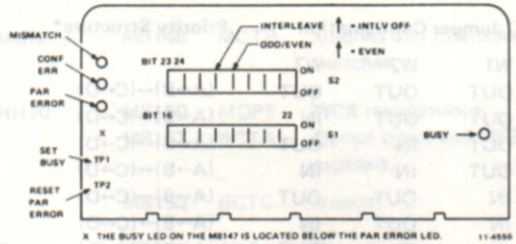
   - *Not Interleaved*
     a. Count the multiples of 32K below this box.
     b. Insert that binary number in the starting address switches.

   - *Interleaved*
     a. Same as above, but both boxes must have same starting address and amount of memory.
     b. Set the Interleave switch for INTLV on both boxes.
     c. Set the ODD/EVEN switch to EVEN on the first box and to ODD on the second box.

16K Modules		32K Modules
M8148	Controller	M8147*
M8149	Transceiver	M8149
G114	Sense/INH	G116
G235	Drive	G236
H217C	Stack	H224C
7010497	Backplane	7010497 with ECO - 04

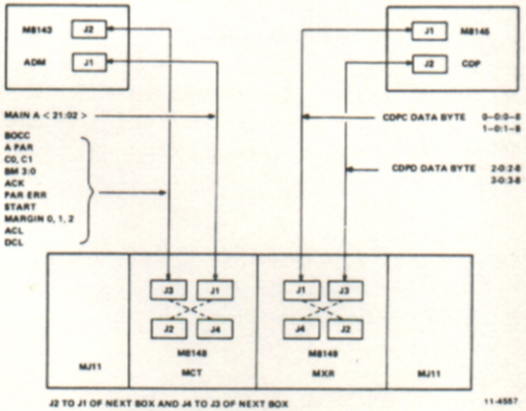
*M8147 will work with 16K and/or 32K stacks.

MJ11 MEMORY STARTING ADDRESS AND INTERLEAVING SWITCHES (M8148)



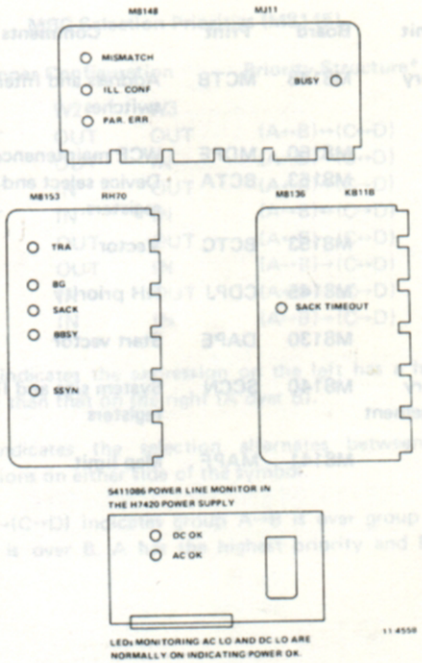
X THE BUSY LED ON THE M8147 IS LOCATED BELOW THE PAR ERROR LED. 11-4556

MJ11 MEMORY CABLING



J2 TO J1 OF NEXT BOX AND J4 TO J3 OF NEXT BOX
AND J2 AND J4 TERMINATED ON LAST BOX OF MEMORY. 11-4557

PDP-11/70 LEDs



LEDs MONITORING AC LO AND DC LO ARE NORMALLY ON INDICATING POWER OK.